## REMARKS

Claims 1-11 are pending in this application. The Examiner rejects claims 1-7 and 9-11 under 35 U.S.C. § 102(b) as being anticipated by Nakano et al. (Nakano), and claim 8 under 35 U.S.C. § 103(a) as being unpatentable over Nakano in view of IEEE Publication, "Hardware-in-the-Loop Simulation Testing and its Integration into a CACSD Toolset", by H. Hanselmann (Hanselmann). Also, the Examiner rejects claims 1-11 under 35 U.S.C. § 112, second paragraph, as being indefinite (see Office Action, paragraph 8). Finally, the Examiner objects to the specification and claims due to various informalities (see Office Action, paragraphs 4-7)

With regard to the Examiner's objections to the specification and claims, as well as the §112, second paragraph, rejection, Applicant amends the specification and the claims as set forth above, and respectfully requests the Examiner to withdraw these objections and rejection accordingly. Applicant notes that the claim amendments are intended to further clarify the claimed invention, and do not narrow the scope of the original claims. No estoppel is created

With regard to the prior art rejections, Applicant respectfully traverses these rejections as follows.

Applicant's claimed invention provides a method and an apparatus (for testing the operation of an electronic unit by simulation) which comprise unique combinations of method steps (claims 1-4) and features (claims 5-10; see also claim 11), including, *inter alia*, processing at least some of the signals output by an electronic unit under test by a programmable logic circuit, storing the values of the parameters corresponding to the signals processed by the programmable logic circuit, and accessing the stored parameters by the simulator's

microprocessor at a frequency which is compatible with the operating frequency of the simulator's microprocessor (see Applicant's independent claims 1 and 5).

Applicant's specification sets forth the following non-limiting examples of implementations of Applicant's claimed invention. According to one embodiment, a simulator 11 is provided with at least one programmable logic circuit 18, and associated buffer memory 19, which interrogates in real time fast signals $S_1$ output from an electronic unit 1 under test without disturbing the operation of a central microprocessor 14 of the simulator 11, whereby the central processor does not require high computational power (see Applicant's specification, pages 8 and 9, and Fig. 1). According to another embodiment, simulator 11 includes an additional programmable logic circuit 28, and associated buffer memory 29, (either stand-alone or integrated as one unit with circuits 18 and 19) for processing of fast signals $E'_1$ output either from central microprocessor 14, or directly from circuit 18 (via link 38), whereby simulations of variation in signal $E_1$ may be performed while microprocessor 14 is dedicated to performing computation operations (see Applicant's specification, pages 9 and 10, and Fig. 3).

Nakano does not disclose, teach or suggest the features of Applicant's invention as claimed in the independent claims 1 and 5.

Nakano provides a method and an apparatus for time correlating internal information of a computer under test with input and output signals of the computer (*see Id.*, Abstract). In particular, Nakano discloses an engine control simulator 20 for analyzing the operating conditions of the ECU 14 for controlling an engine 12 mounted onto a motor vehicle 10 where:

> in storing the internal information of the computer [i.e., computer of ECU 14], which is stored in the random access memory, the register and the like

> together with the input and output signals of the computer and indicating the same, the internal information of the computer, which is added thereto with the time information, at which the internal information is read out, is stored, and the input and output signals of the computer are synchronized with the time information to indicate the internal information, so that the changes of the internal information corresponding to the changes of the input and output signals, can be indicated in synchronism with each other. In consequence, the operating conditions of the computer can be properly analyzed. (*Id.*, col. 6, lines 10-24; *see also Id.*, col. 8, line 31 through col. 13, line 57)

Contrary to the Examiner's analysis, nowhere does Nakano disclose, teach or suggest accessing stored parameters corresponding to signals output by ECU 14 at a frequency which is compatible with the operating frequency of the microprocessor of its simulator 20. In fact, Nakano has nothing to do with access frequency, let along access frequency of stored parameters corresponding to signals output by units under test, as recited in Applicant's independent claims 1 and 5. Instead, Nakano simply provides a process and a method where "input and output signals of the computer [under test] are synchronized with the time information to indicate the internal information [of the computer under test], so that the changes of the internal information corresponding to the changes of the input and output signals, can be indicated in synchronism with each other" (*see Id.*, col. 6, lines 17-22).

Therefore, Applicant's independent claims 1 and 5, as well as their respective dependent claims 2-4, 6, 7 and 9-11 (which incorporate all the novel and unobvious features of their respective base claims), are not anticipated by (i.e., are not readable on ) Nakano at least for these reasons.

With regard to the dependent claim 8, Hanselmann discloses nothing more than a general concept of HIL simulation testing, and does not supply the above-noted deficiency of Nakano.

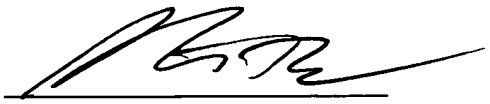
Therefore, Applicant's dependent claim 8 (which incorporate all the novel and unobvious features of its base claim 5) would not have been obvious from any reasonable combination of Nakano and Hanselmann at least for the reasons set forth above with respect to claims 1 and 5.

In view of the above, reconsideration and allowance of this application are now believed to be in order, and such actions are hereby solicited. If any points remain in issue which the Examiner feels may be best resolved through a personal or telephone interview, the Examiner is kindly requested to contact the undersigned at the telephone number listed below.

Finally, as a formal matter, Applicant notes that, while the Examiner indicates that he has considered all of the references submitted with Applicant's IDS filed August 30, 2000 (see Office Action, paragraph 2), the Examiner did not initial one of the references listed on a copy of the corresponding Form 1449 attached to the Office Action. Thus, Applicant requests the Examiner to correct this apparent oversight in the next Office correspondence.

The USPTO is directed and authorized to charge all required fees, except for the Issue Fee and the Publication Fee, to Deposit Account No. 19-4880. Please also credit any overpayments to said Deposit Account.

Respectfully submitted,



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